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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATITORNEY DOCKET NO.	CONFIRMATION NO.	
10/073,312	02/13/2002	Tetsuo Sasaki	ASA-1062	4469	
7	590 08/25/2004		EXAMINER		
Mattingly, Stranger & Malur, P.C.			DIMYAN,	DIMYAN, MAGID Y	
Suite 370 1800 Diagonal Road Alexandria, VA 22314			ART UNIT	PAPER NUMBER	
			2825		
	DATE N		DATE MAILED: 08/25/200	4	

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)	
Office Action Summany	10/073,312	SASAKI ET AL.	
Office Action Summary	Examiner	Art Unit	ل ما
	Magid Y Dimyan	2825	Par 1
The MAILING DATE of this communication app Period for Reply	pears on the cover sheet with the (correspondence ad	dress
A SHORTENED STATUTORY PERIOD FOR REPL' THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.1 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a repl' - If NO period for reply is specified above, the maximum statutory period of Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be ting within the statutory minimum of thirty (30) day will apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	mely filed ys will be considered timely the mailing date of this co	
Status			
1) Responsive to communication(s) filed on 30 Ju	<u>une 2004</u> .		
2a)⊠ This action is FINAL . 2b)□ This	action is non-final.	•	
3) Since this application is in condition for alloward closed in accordance with the practice under E	· · · · · · · · · · · · · · · · · · ·		e merits is
Disposition of Claims			
4) ☐ Claim(s) 1-15 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) ☐ Claim(s) _ is/are allowed. 6) ☐ Claim(s) 1-3 and 8 is/are rejected. 7) ☐ Claim(s) 4-7 and 9-15 is/are objected to. 8) ☐ Claim(s) are subject to restriction and/o	wn from consideration.		
Application Papers			
9)☐ The specification is objected to by the Examine	er.		
10)⊠ The drawing(s) filed on 13 February 2002 is/are	e: a)⊠ accepted or b)⊡ objecte	d to by the Examir	ner.
Applicant may not request that any objection to the			
Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Ex	,	•	, ,
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority application from the International Bureau * See the attached detailed Office action for a list	s have been received. s have been received in Applicati rity documents have been receive u (PCT Rule 17.2(a)).	ion No ed in this National	Stage
Attachment(s) Notice of References Cited (PTO-892)	4) Interview Summary	(PTO 442)	
Notice of References Cited (PTO-992) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	Paper No(s)/Mail D	ate)-152)

DETAILED ACTION

Acknowledgement

1. Receipt is acknowledged to the Amendments, and to the Remarks, in response to the Office Action. Both were filed on June 30, 2004. It is also acknowledged that the amendments made to the specification and to the claims were acceptable to the Examiner to overcome the objections and the 35 USC § 112 rejections cited by the Examiner in the First Office Action. Other grounds for objections to the claims have been found. Also, the arguments made by the Applicants in their Remarks were not persuasive to the Examiner, in order to traverse the 35 USC § 102 rejections of Claims 1 – 3 and 8 of the Office Action as recited below.

Claim Objections

2. Claims 1, 3, 4, 5, 7, 9,10, 11, 12, 13, 14 and 15 objected to because of the following informalities: the claims are replete with incomprehensible elements as described, and require more understandable language. Below are some examples, but the Applicants are requested to thoroughly check and correct all the deficient claim language:

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- Claim 1, line 17, delete "said", and insert --each--. Also, the Examiner does not understand the meaning of "requirement of each flop-flop" (lines 18 and 19 in claim 1). There is no previous mention of "flip-flop requirements".

- Claim 3, line 2; the Examiner fails to determine whether "said *method*" refers to "*method of designing*", or "*method of adjusting clock timing*".
- Claim 4, lines 3 4, delete "said method provides clock timing of each flip-flop,
 and", and insert --the clock timing of each flip-flop extracts--.
- Claim 4, lines 9 13; the Examiner does not understand the meaning of the last statement in the claim "from among clock timing that said each flip-flop...". The Applicants are requested to elucidate.
- Claims 5, 10 and 14 do not make sense to the Examiner, and thus require further clarification and restating.
- Claim 7, line 3, delete "said method determines the clock timing of each flip-flop" and insert --the clock timing of each flip-flop is determined--.
- Claim 9, line 11, "adjusting costs by the adjusting methods" is missing a verb between "costs" and "by". Also, the Examiner does not understand the

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meaning of the entire limitation described on lines 12 – 16 ("target machine cycles").

- Claim 12 contains the same issues as claim 12, and thus the same objections apply.
- The Examiner does not understand the meaning of the last statement in claim 15, lines 13 – 18 (... and a first path along which data transmission is impossible in said target machine cycle...). A restatement of that element is requested.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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Claims 1 – 3 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by
 U.S. Patent No. 6,367,060 to Cheng et al (hereinafter, Cheng).

- 2. Referring to claim 1, Cheng cites a method for designing an IC consisting of (a) dividing the chip into a number of clusters (i.e., areas) and providing clock pins in these clusters (see column 2, lines 1 27; column 5, lines 48 52); (b) performing clock signal distribution from a clock source to each of the clusters (see Fig. 5); (c) performing adjustment of clock timing for each flip-flop to flip-flop transmission to meet system clock frequency requirements (see Fig. 5; column 9, lines 12 24); and (d) balancing the timing by balancing the flip-flops via grouping them together (Figs. 4 and 5; column 4, line 30 to column5, line 67). Thus, Cheng recites all the elements claimed herein.
- 3. As per claim 2, see column 4, lines 46 48; column 10, lines 17 19, which show how the length of a transmission path (i.e., extending wiring length) can affect the propagation delays (i.e., can be used to adjust timing) as claimed herein.
- 4. Referring to claim 3, see (6) and (7) above, as well as column 4, lines 38 45; column 3, lines 38 67, which recite other ways of adjusting timing, as claimed.
- 5. As for claim 8, see (6) above, as well as Fig. 6; column 7, line 59 to column 10, line 33, which recite all the elements of the claim, including means for adjusting clock

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timing and means for displaying signal propagation paths (closed loops), as claimed herein.

Allowable Subject Matter

- 6. Claims 9 15 are allowable if rewritten to overcome the objections cited above.
- 7. Claims 4-7 are objected to as being dependent upon a rejected base claim, but would be allowable if: (a) rewritten in independent form including all of the limitations of the base claim and any intervening claims; and (b) rewritten to overcome the objections cited above.
- 8. The following is a statement of reasons for the indication of allowable subject matter: these claims pertain to a method of designing an IC that include timing elements and relationships for determining flip-flip to flip-flop path delays that are not disclosed in the references of record.
- 9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Response to Arguments

10. Applicant's arguments filed June 30, 2004 have been fully considered but they are not persuasive. As for the argument that the current application discloses a method of designing an IC in which a chip is divided into a number of areas with a plurality of clock pins provided for each area, Cheng teaches a method of designing an IC in which a chip is divided into a number of balanced "clusters" (i.e., a number of areas). Furthermore, these balanced (defined) clusters contain the clock pins that drive the flip-flops thereby permitting the circuit to be designed with a minimum of delay fluctuations (see Fig. 4; col. 4, lines 20 – 55). As for the argument that the present invention establishes and chooses from a plurality of methods of adjusting clock signal timing,

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Cheng teaches using more than one design constraint to balance (adjusts) clock timing (see col. 2, lines 1-27), thus rendering all of the Applicants' arguments moot.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

ANNETTE A THOMPSON-PRIMARY EXAMINER Magid Y Dimyan Examiner Art Unit 2825

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myd 20 August 2004